WHAT IS CLAIMED IS:

1. A protocol data unit switching method that implements switching means used for the selective interconnection of a transmitter port and at least one receiver port selected from among at least two receiver ports by means of at least one internal bus, each of the protocol data units being constituted by at least one elementary piece of data,
wherein the method implements:

- a synchronization mechanism defining time slots, known as connection cycles, on at least one of said internal buses;

- a mechanism for the allocation of at least one of said connection cycles to each of the selected receiver ports; and

- a mechanism for the writing of at least one piece of elementary data in the allocated connection cycle or cycles so as to enable the broadcasting of elementary data to said selected receiver ports.

2. A method according to claim 1, wherein said writing mechanism comprises a verification step determining whether each of said pieces of elementary data has been received by each of the selected receiver ports.

3. A method according to claim 2, wherein said mechanism for writing elementary data in each of the allocated connection cycles is reiterated so long as the piece of elementary data has not been received by all the receiver ports.

4. A method according to any of the claims 1 to 3, wherein said allocation mechanism comprises a step of association of each of said connection cycles to each of said selected receiver ports.

5. A method according to any of the claims 1 to 4, wherein said allocation mechanism comprises:

- a step for the detection of a transmitter port requesting the transfer of at least one protocol data unit towards at least one selected receiver port;

- a step for verifying that the selected receiver ports or ports are ready to receive the protocol data unit or units; and

- a step for the validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected

receiver ports during the validated connection cycle or cycles when the verification is positive.

6. A method according to any of the claims 1 to 5, implementing at least one first input bus multiplexing the elementary data coming from at least two transmitter ports and/or at least one first output bus multiplexing said elementary data addressed to at least two receiver ports.

7. A method according to any of the claims 1 to 6, wherein said transmitter and receiver ports are organized in pairs each combining a transmitter port and a receiver port, each pair being associated with a distinct link.

8. A method according to any of the claims 1 to 7, implementing at least one link connected to transmitter ports and/or to receiver ports.

9. A method according to claim 8, wherein the link belongs to the group comprising:

- the IEEE 1355 or equivalent links; and
- the external buses.

10. A method according to any of the claims 1 to 9, wherein said method is capable of switching data whose bit rate is greater than or equal to 100 Mbits/s.

11. A method according to any of the claims 1 to 10, wherein said writing mechanism comprises at least one step for the writing of each piece of elementary data of each said protocol data units, each of said steps for writing each piece of elementary data comprising:

- a sub-step for the acceptance, by each of said selected receiver ports, of the writing of each piece of elementary data to be transmitted; and
- a sub-step for the transmission of said each piece of elementary data to be transmitted, to each of said selected receiver ports.

12. A method according to claim 11, wherein during said acceptance stage, the acceptance is conditioned by a degree of filling of a reception memory associated with said selected receiver port, for each of said receiver ports.

13. A method according to any of the claims 1 to 12, wherein said writing mechanism comprises at least one step of arbitration for at least one bus

connecting a set of at least one input port comprising said transmitter port to a set of at least one output port comprising said receiver ports, said arbitration step being carried out by a switching matrix consisting of crosspoints capable of transmitting elementary data between an input port and an output port, and being organized in rows and columns,

- each column (or row respectively) being capable of managing the reception of elementary data coming from an input port associated with the column (or row respectively); and

- each row (or column respectively) being capable of managing the transmission of elementary data to an output port associated with the row (or column respectively);

so that a single crosspoint per row (or column respectively), at a given point in time, can enable the transmission of elementary data.

14. A method according to any of the claims 1 to 13, wherein each protocol data unit transmitted comprises at least one header and wherein the method furthermore comprises:

- at least one step for the analysis of said header; and/or

- at least one step for the modification of said header.

15. A protocol data unit switching device implementing switching means to selectively interconnect a transmitter port and least one receiver port selected from at least two receiver ports by means of at least one internal bus, each of the protocol data units being formed by at least one piece of elementary data, wherein the device implements:

- a synchronization means defining time slots, known as connection cycles, of at least one of said internal buses;

- a means for the allocation of at least one of the connection cycles to each of the selected receiver ports; and

- a means of writing at least one piece of elementary data in the allocated connection cycle or cycles, so as to enable the broadcasting of said elementary data to the selected receiver ports.

16. A device according to claim 15, wherein said writing means comprises a verification means determining whether each of said pieces of elementary data has been received by each of the selected receiver ports.

17. A device according to claim 16, wherein said means for writing the elementary data in each of the allocated connection cycles is implemented so long as the piece of elementary data has not been received by all the receiver ports.

18. A device according to any of the claims 15 to 17, wherein said allocation mechanism comprises a step of association of each of said connection cycles to each of said selected receiver ports.

19. A device according to any of the claims 15 to 18, wherein said allocation mechanism comprises:

- a means for the detection of a transmitter port requesting the transfer of at least one protocol data unit towards at least one selected receiver port;

- a means for verifying that the selected receiver ports or ports are ready to receive the protocol data unit or units; and

- a means of validation of at least one connection cycle used for the writing of the elementary data of the protocol data unit or units in the selected receiver ports during the validated connection cycle or cycles when the verification is positive.

20. A device according to any of the claims 15 to 19, implementing at least one first input bus multiplexing the elementary data elements coming from at least two transmitter ports and/or at least one first output bus multiplexing the pieces of elementary data addressed to at least two receiver ports.

21. A device according to any of the claims 15 to 20, wherein said transmitter and receiver ports are organized in pairs each combining a transmitter port and a receiver port, each pair being associated with a distinct link.

22. A device according to any of the claims 15 to 21, implementing at least one link connected to transmitter ports and/or to receiver ports.

23. A device according to claim 22, wherein the link belongs to the group comprising:

- the IEEE 1355 or equivalent links; and

- the external buses.

24. A device according to any of the claims 15 to 23, wherein said device is capable of switching data whose bit rate is greater than or equal to 100 Mbits/s.

25. A device according to any of the claims 15 to 24, wherein said writing means implements a step for the writing of each piece of elementary data of each of said protocol data units, and itself comprises:

- a means for the acceptance, by each of the selected receiver ports, of the writing of said each piece of elementary data to be transmitted, and

- a means for the transmission of said each piece of elementary data to be transmitted, to each of the selected receiver ports.

26. A device according to claim 25, wherein the acceptance implemented by said acceptance means is conditioned by a degree of filling of a reception memory associated with the selected receiver port, for each of said receiver ports.

27. A device according to claim 26, wherein said memory comprises at least one FIFO.

28. A device according to any of the claims 15 to 27, wherein said writing means comprises at least one arbitration means of at least one bus connecting a set of at least one input port comprising said transmitter port to a set of at least one output port comprising said receiver ports, the arbitration step being carried out by a switching matrix consisting of crosspoints capable of transmitting elementary data between an input port and an output port, and organized in rows and columns,

- each said column (or row respectively) being capable of managing the reception of elementary data coming from an input port associated with the column (or row respectively); and

- each said row (or column respectively) being capable of managing the transmission of elementary data to an output port associated with the row (or column respectively);

so that a single crosspoint per row (or column respectively), at a given point in

time, can enable the transmission of pieces of elementary data.

29. A device according to any of the claims 15 to 28, wherein each protocol data unit transmitted comprises at least one header and the method furthermore comprises:

- at least one means for the analysis of said header; and/or
- at least one means for the modification of said header.

30. A device according to any of the claims 15 to 29, furthermore comprising an interfacing means delivering, to a control module and through a clock signal transmission means, clock signals regenerated from packets received by said interfacing means.

31. A device according to any of the claims 15 to 29, furthermore comprising an interfacing means transmitting and/or receiving information through at most two connection buses addressed to and/or coming from at least one of the means belonging to the group comprising said synchronization means, said allocation means and said writing means.

32. A device according to claim 31, wherein the protocol data units sent out by at least one emitter port towards FIFOs are multiplexed by a reception linking bus.

33. A device according to any of the claims 31 and 32, wherein the protocol data units received by at least one receiver port through the FIFOs are demultiplexed on a transmission linking bus.

34. A switching apparatus comprising:

- at least one switching device according to any of the claims 15 to 33,
- and at least one element belonging to the group comprising:
  - the IEEE 1355 or equivalent links, and
  - the external buses.

35. A switching apparatus according to claim 34, connected to a data-processing apparatus.

36. An application of the method according to any of the claims 1 to 14 to at least one of the fields belonging to the group comprising:

- high bit rate switching;
- distributed applications;
- the transmission of digital data;
- the reception of digital data;
- audio applications;
- company networks; and
- real-time image transmission.

37. A computer program product wherein the program comprises instruction sequences matched to the implementation of a method according to any of the claims 1 to 14, when the program is executed by computer.

38. A computer program product for the switching of protocol data units implementing switching means for the selective interconnection of a transmitter port and at least one receiver port selected from at least two receiver ports by means of at least one internal bus, each of the protocol data units being constituted by at least one piece of elementary data, the computer program product comprising program code instructions recorded on a carrier that can be used in a computer comprising:

- programming means readable by computer to carry out a synchronization step defining time slots, known as connection cycles, on at least one of the internal buses;

- programming means readable by computer to carry out a step for the allocation of at least one of the connection cycles to each of said selected receiver ports and

- programming means readable by computer to carry out a writing step for the writing of at least one piece of elementary data in the allocated connection cycle or cycles so as to enable the broadcasting of said elementary data to said selected receiver ports.